ABSTRACT OF THE DISCLOSURE

An integrated overvoltage and reverse voltage protection circuit that includes two p-channel double-sided extended drain transistors coupled to a high voltage source, each having their n-well coupled through a resistor to the high voltage source. For voltage regulation, a voltage divider is coupled in series with a first of these transistors, while the drain of the second transistor is coupled to the gate of the first transistor. For voltage blocking, the voltage divider may span the entire supply voltage. An n-channel transistor couples the second p-channel transistor to a low voltage source. A middle node in the voltage divider is coupled to one input of a comparator, with a reference voltage coupled to the second input. The comparator output drives the gate terminal of the n-channel transistor. A load to be protected may be disposed in parallel with the voltage divider.

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